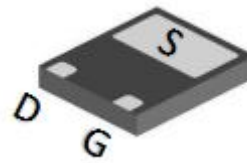


Features

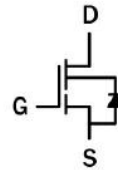
- 650V, 9A, $R_{DS(on)}$ (typ.) = 180mΩ@VGS = 12V.
- Very low Q_{RR}
- Reduced Crossover Loss
- Easy to drive with commonly-used gate drivers
- Excellent $Q_G \times R_{DS(on)}$ figure of merit (FOM)
- RoHS compliant and Halogen-free

Application

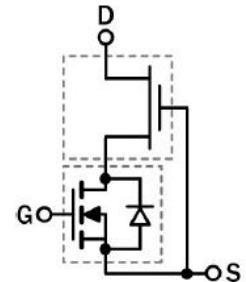
- High efficiency power supplies
- High efficiency USB PD adapters
- Other consumer electronics



DFN5*6
Bottom View



Cascode Schematic Symbol



Cascode Device Structure

Absolute Maximum Ratings (T_C = 25° C unless otherwise noted)

Symbol	Parameter		Limit	Unit
V _{DS}	Drain-Source Voltage		650	V
V _{(TR)DSS}	Transient Drain to Source Voltage ^a		800	V
V _{GSS}	Gate-Source Voltage		± 20	V
I _D	Drain Current-Continuous	T _C = 25°C ^b	9	A
	Drain Current-Continuous	T _C = 100°C ^b	5.7	A
I _{DM}	Drain Current-Pulsed	Pulse Width = 100μs	30	A
P _D	Maximum power Dissipation @T _C = 25°C		28	W
T _C	Operating Temperature Case		-55 to +150	°C
T _J	Operating Temperature Junction		-55 to +150	°C
T _S	Storage Temperature		-55 to +150	°C
T _{SOLD}	Soldering Peak Temperature ^c		260	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
R _{θJC}	Thermal Resistance Junction-Case	4.5	°C/W
R _{θJA}	Thermal Resistance Junction-Ambient ^d	50	°C/W

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

■ Off Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{(BL)DSS}$	Reverse Breakdown Voltage	$V_{GS} = 0V$	650	-	-	V
I_{DSS}	Reverse Leakage Current	$V_{GS} = 0V, V_{DS} = 650V$ $T_J = 25^\circ\text{C}$	-	-	20	μA
		$V_{GS} = 0V, V_{DS} = 650V$ $T_J = 150^\circ\text{C}$	-	50	-	μA
I_{GSS}	Gate-to-source Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 150	nA

■ On Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 500\mu\text{A}$	3	4	5	V
$R_{DS(on)eff}$	On Resistance	$V_{GS} = 12V, I_D = 4A$ $T_J = 25^\circ\text{C}$	-	180	225	m Ω
		$V_{GS} = 12V, I_D = 4A$ $T_J = 150^\circ\text{C}$	-	360	-	

■ Dynamic Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
C_{ISS}	Input Capacitance	$V_{GS} = 0V,$ $V_{DS} = 400V$ $f = 1\text{MHz}$	-	331	-	pF
C_{OSS}	Output Capacitance		-	21	-	
C_{RSS}	Transfer Capacitance		-	0.7	-	
$C_{o(er)}$	Output Capacitance, energy related	$V_{GS} = 0V,$ $V_{DS} = 0 \sim 400V$	-	32	-	pF
$C_{o(tr)}$	Output Capacitance, time related		-	81	-	
Q_{OSS}	Output Charge		-	33	-	nC

■ On Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 0 \sim 12V,$ $V_{DS} = 400V,$ $I_D = 5.7A,$ $R_g = 47\Omega$	-	50	-	ns
t_r	Turn-On Rise Time		-	6	-	
$t_{d(off)}$	Turn-Off Delay Time		-	80	-	
t_f	Turn-Off Fall Time		-	5	-	
Q_G	Total Gate Charge	$V_{GS} = 0 \sim 12V,$ $V_{DS} = 400V,$ $I_D = 5.7A$	-	7.6	-	nC
Q_{GS}	Gate-Source Charge		-	2.2	-	
Q_{GD}	Gate-Drain Charge		-	2.8	-	



MGY23N65H

650V GaN Power Transistor (FET)

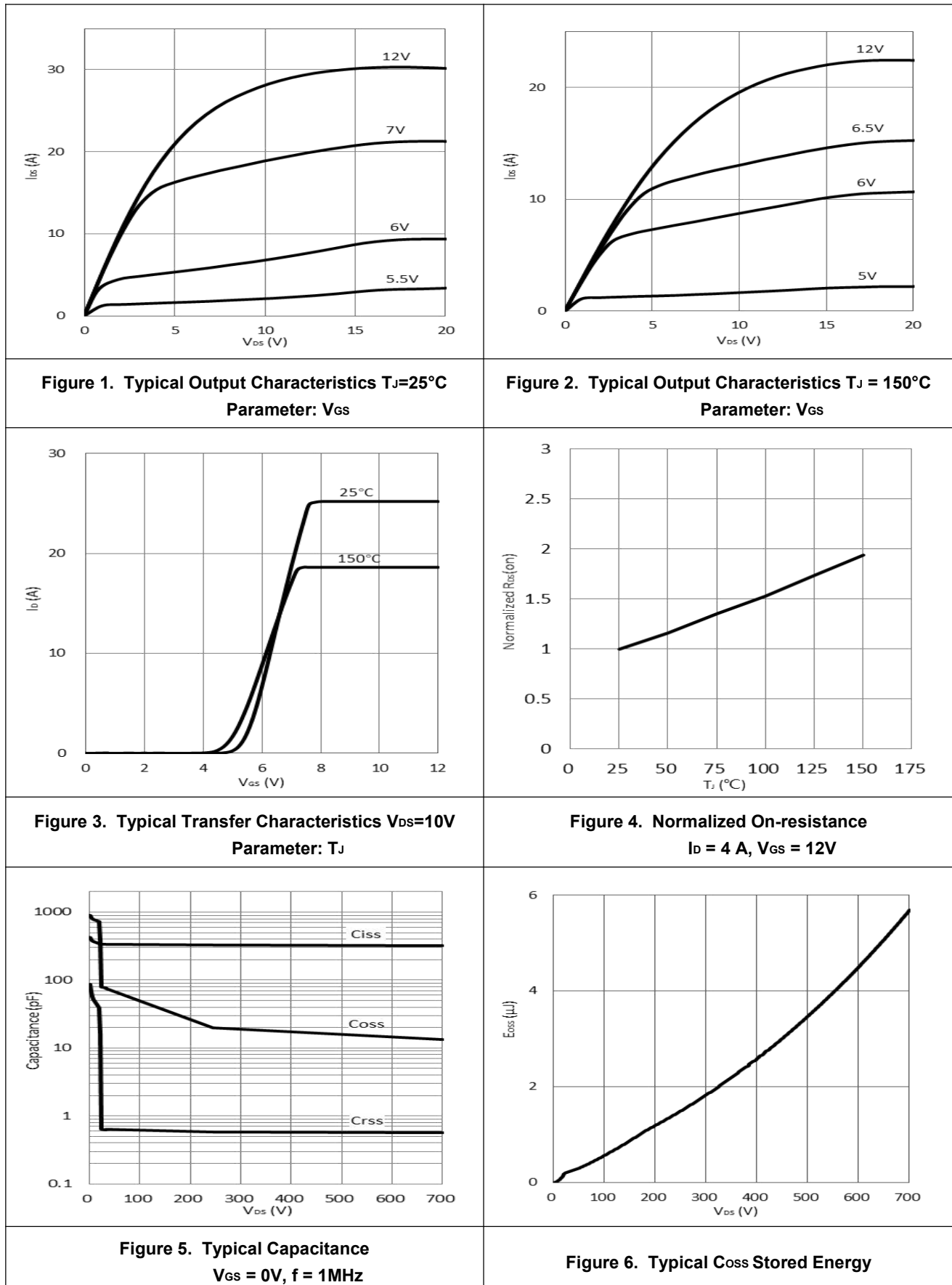
■ Drain-Source Diode Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{SD}	Reverse Voltage	$V_{GS} = 0V, I_S = 3 A$	-	1.3	-	V
		$V_{GS} = 0V, I_S = 6 A$	-	1.9	-	V
t_{RR}	Reverse Recovery Time	$I_S = 6 A, V_{DS} = 400V,$ $di/dt = 1000 A/\mu s$	-	18	-	ns
Q_{RR}	Reverse Recovery Charge		-	33	-	nC

Notes:

- In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu s$.
- For increased stability at high current operation.
- Reflow MSL3.
- Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with $6cm^2$ copper area and $70\mu m$ thickness).

Typical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)



Typical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

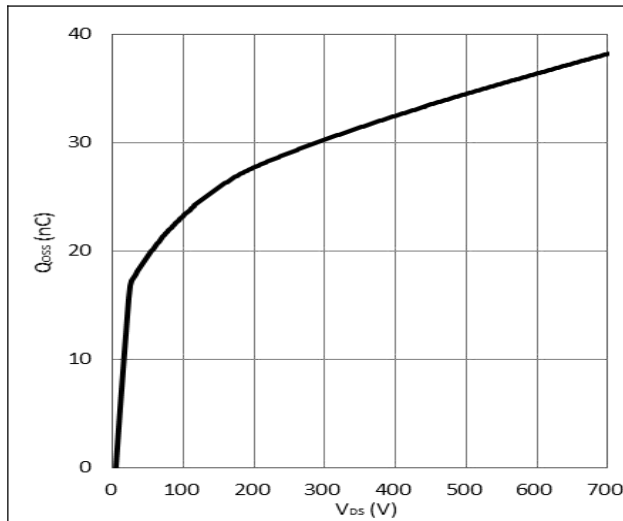


Figure 7. Typical Q_{oss}

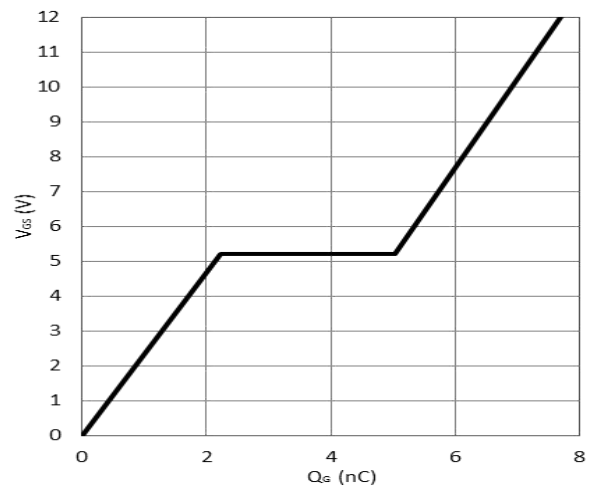


Figure 8. Typical Gate Charge

$I_{DS} = 5.7\text{A}$, $V_{DS} = 400\text{V}$

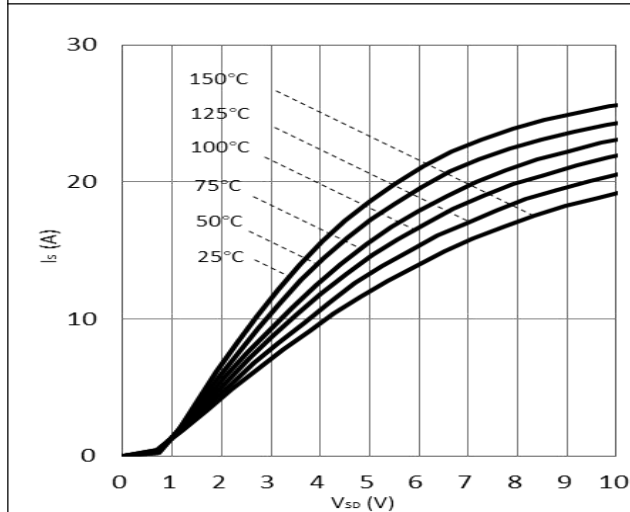


Figure 9. Forward Characteristics of Rev.

Diode $I_s = f(V_{sd})$, Parameter T_j

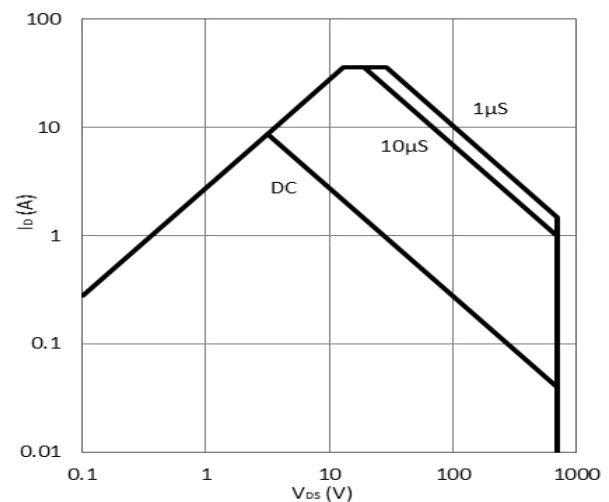


Figure 10. Safe Operating Area $T_c = 25^\circ\text{C}$

(calculated based on thermal limit)

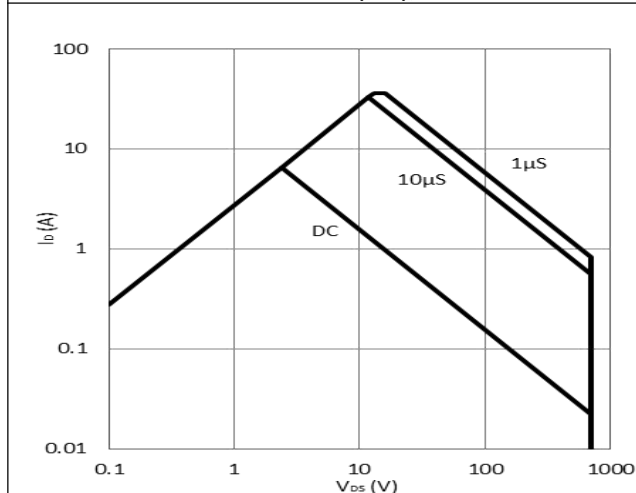


Figure 11. Safe Operating Area $T_c = 80^\circ\text{C}$

(calculated based on thermal limit)

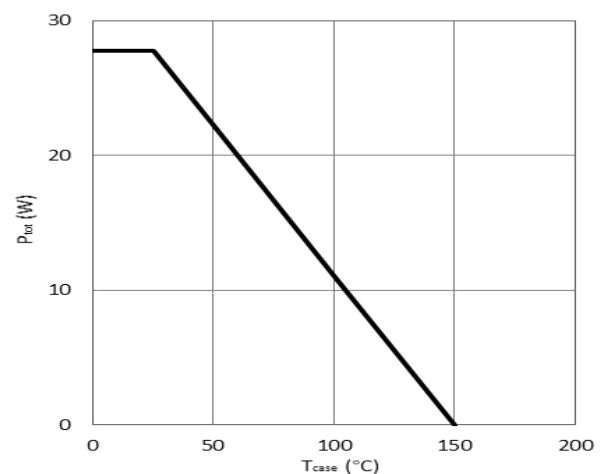


Figure 12. Power Dissipation

Typical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

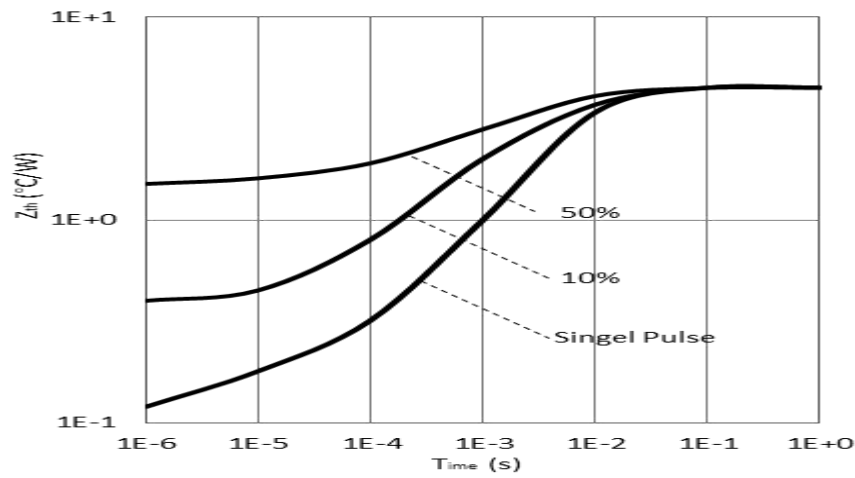


Figure 13. Transient Thermal Resistance

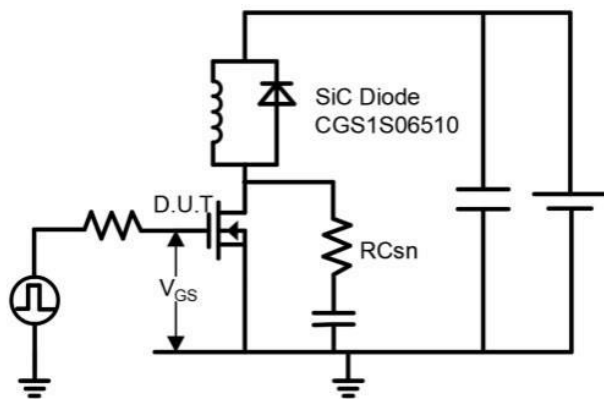


Figure 14. Switching Time Test Circuit

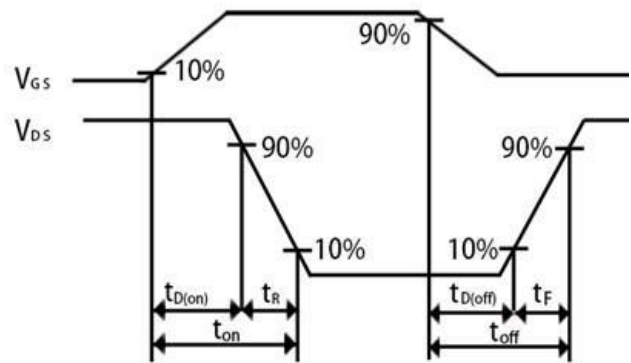


Figure 15. Switching Time Waveform

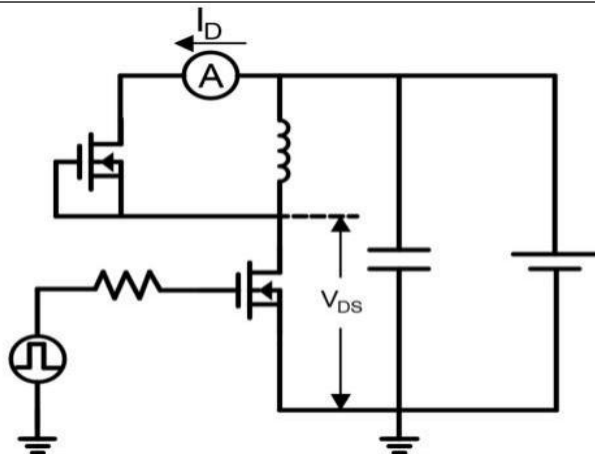


Figure 16. Diode Characteristics Test Circuit

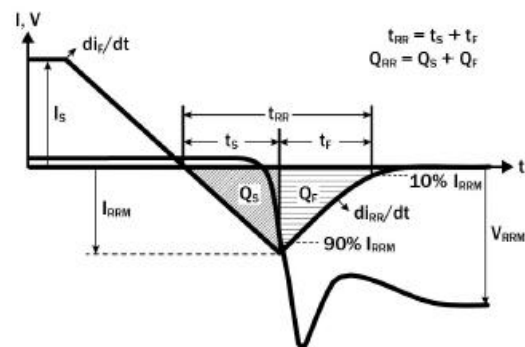
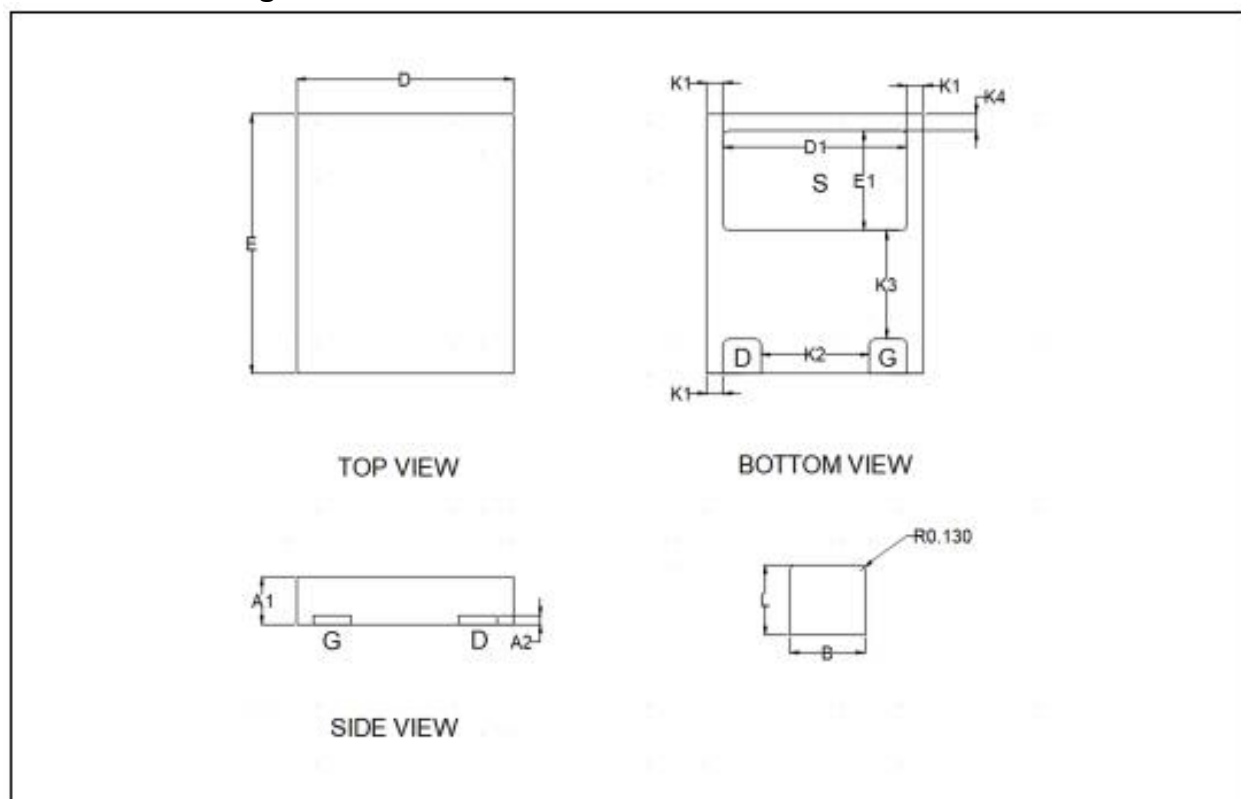


Figure 17. Diode Recovery Waveform

■ DFN5*6 Package Information



SYMBOL	Millimeter		
	Min	Nom	Max
A1	0.80	0.90	1.15
A2	0.19	0.20	0.22
B	0.82	0.87	0.92
D	4.90	5.00	5.10
E	5.90	6.00	6.10
D1	4.09	4.23	4.39
E1	2.15	2.30	2.45
L	0.71	0.81	0.91
K1	0.28	0.38	0.48
K2	2.40	2.50	2.60
K3	2.40	2.50	2.60
K4	0.29	0.39	0.49



MGY23N65H

650V GaN Power Transistor (FET)

■ Revision History

Version	Date	Subjects (major changes since last revision)
0.1	2023-05-07	Preliminary Version
1.0	2024-10-10	Datasheet Complete